In the claims:

For the Examiner's convenience, all pending claims are presented below with changes shown.

1. (Currently Amended) A computer system comprising:

a main memory device; and

a memory controller, coupled to the main memory device, including:

a first queue to store packets that are to be transmitted from the memory controller to the main memory device;

a scheduler ~~that includes a slot-based controller, wherein the slot-based controller is adaptable~~ to launch a first packet from the first queue that straddles a first fixed packet slot and a second fixed packet slot.

2. (Currently Amended) The computer system of claim 1 wherein the ~~packet~~ launch position of the first packet is advanced one half of a slot position relative to the second fixed packet slot.

3. (Currently Amended) The computer system of claim 1 wherein the first packet is tagged with an attribute that indicates that the packet is straddling the first fixed packet slot and the second fixed packet slot.

4. (Original) The computer system of claim 3 wherein the attribute is a Rambus clock offset.

5. (Currently Amended) The computer system of claim 1 wherein the first packet is a Rambus control packet.

6. (Currently Amended) The computer system of claim 1 wherein the memory controller further comprises a Rambus Asic Cell (RAC)~~, wherein the RAC interfaces~~ to interface with the main memory device via a high frequency expansion channel.

7. (Currently Amended) The computer system of claim 6 wherein the memory ~~slot-based~~ controller further comprises:

~~a scheduler;~~

a rules checker coupled to the scheduler;

~~a future packet queue coupled to the scheduler and the rules checker;~~ and

a ~~past packet~~ second queue coupled to the ~~future packet~~ first queue, the scheduler and the rules checker.

8. (Currently Amended) The computer system of claim 7 ~~6~~ wherein the rules checker uses entries in the ~~past packet~~ second queue to validate future slot choices for the scheduler.

9. (Original) The computer system of claim 7 wherein the ~~past packet~~ second queue and the ~~future packet~~ first queue are unidirectional shift registers.

10. (Currently Amended) The computer system of claim 7 wherein the memory ~~slot-based~~ controller further comprises packet driving logic coupled to the RAC and the scheduler to interface with the RAC.

11. (Currently Amended) The computer system of claim 6 wherein the memory controller further comprises~~comprising~~:

an expansion channel coupled to the RAC~~within the memory controller; and~~

~~a repeater coupled to the expansion channel~~.

12. (Currently Amended) The computer system of claim 11 wherein the main memory device comprises~~further comprising~~:

a repeater coupled to the expansion channel;

a stick channel coupled to the repeater; and

a plurality of memory devices coupled to the stick channel.

13. (Original) The computer system of claim 12 wherein the memory devices are Rambus Dynamic Random Access Memories (RDRAMs).

14. (Original) The computer system of claim 11 further comprising a plurality of memory devices coupled to the expansion channel.

15. (Currently Amended) A memory controller comprising:

a first queue to store packets that are to be transmitted from the memory controller to the main memory device;

a scheduler ~~a slot-based controller adaptable~~ to launch a first packet from the first queue that straddles a first fixed packet slot and a second fixed packet slot.

16. (Currently Amended) The memory controller of claim 15 wherein the first packet launch position is advanced one half of a slot position relative second fixed packet slot.

17. (Currently Amended) The memory controller of claim 15 wherein the first packet is tagged with an attribute that indicates that the first packet is straddling the first fixed packet slot and the second fixed packet slot.

18. (Original) The memory controller of claim 17 wherein the attribute is a Rambus clock offset.

19. (Currently Amended) The memory controller of claim 15 wherein the first packet is a Rambus control packet.

20. (Currently Amended) The memory controller of claim 15 ~~wherein the memory controller~~ further ~~comprises~~ comprising a Rambus Asic Cell (RAC) ~~wherein the RAC interfaces~~ to interface with a main memory device via a high frequency expansion channel.

21. (Currently Amended) The memory controller of claim 20 wherein the slot-based controller comprises:

~~a scheduler;~~

a rules checker coupled to the scheduler;

~~a future packet queue coupled to the scheduler and the rules checker;~~ and

a ~~past packet~~ second queue coupled to the ~~future packet~~ first queue, the scheduler and the rules checker.

22. (Currently Amended) The memory controller of claim 21 wherein the rules checker uses entries in the ~~past packet~~ second queue to validate future slot choices for the scheduler.

23. (Currently Amended) The memory controller of claim 21 wherein the ~~past packet~~ second and the ~~future packet~~ first queue are unidirectional shift registers.

24. (Original) The memory controller of claim 21 wherein the slot-based controller further comprises packet driving logic coupled to the RAC and the scheduler.

25. (Currently Amended) A method ~~slot-based controller~~ comprising:

~~a scheduler;~~

~~a rules checker coupled to the scheduler;~~

~~a future packet queue coupled to the scheduler and the rules checker; and~~

~~a past packet queue coupled to the future packet queue, the scheduler and the rules checker;~~

~~wherein the slot-based controller is adaptable to launch a packet in advance of a predetermined packet slot.~~

retrieving a first packet from a packet queue; and

transmitting the first packet to a memory, wherein the first packet is transmitted straddling a first fixed packet slot and a second fixed packet slot.

26. (Currently Amended) The ~~slot-based controller~~ method of claim 25 ~~wherein the advance packet launch is accomplished by straddling the packet on a first fixed packet slot and a second fixed packet slot, wherein the first packet slot is designated for a previously scheduled packet.~~ further comprising advancing the launch position of the first packet one half of a slot position relative to the second fixed packet slot.

27. (Currently Amended) The ~~memory controller~~ method of claim 25 ~~wherein the past packet queue and the future packet queue are unidirectional shift registers.~~ further comprising tagging the first packet with an attribute that indicates that the packet is straddling the first fixed packet slot and the second fixed packet slot.

28. (Currently Amended) The ~~memory controller~~ method of claim 25 ~~wherein the slot based controller further comprises packet driving logic coupled to the RAC and the scheduler.~~further comprising accessing a second queue to track previously transmitted packets.